REMARKS/ARGUMENTS

Claims 1-17 and 34 have been examined, with claims 18-33 being directed to a non-elected invention.

Claims 1, 3-5 and 34 have been rejected under 35 USC 102(b) as anticipated by Kawaguchi. Claims 2 and 6-12 have been rejected under 35 USC 103(a) as unpatentable over Kawaguchi. Claims 13-17 have been rejected under 35 USC 103(a) as unpatentable over Kawaguchi in view of Mukai. Reconsideration and withdrawal of these rejections are respectfully requested in view of the claim changes made herein and in light of the following remarks.

Claim 1 has been amended herein to specify that "setting growth parameters used during production of the compound semiconductor layer such that, at least in some cases in a vicinity of dislocations in the compound semiconductor layer, regions are produced in the compound semiconductor layer having a lower thickness than remaining regions of the compound semiconductor layer to build up a shielding energy barrier in the regions having the lower thickness." (emphasis added) This feature is disclosed in the paragraph spanning pages 5 and 6 of the specification and, in particular, on page 5, line 21. Also, this feature is illustrated in Figs. 2 and 3.

The shielding energy barriers which are formed, in accordance with the invention, in the vicinity of dislocations suppress diffusion of charge carriers toward the dislocations and, therefore, prevent possible non-radiating recombinations of electron-hole pairs at these dislocations.

According to Kawaguchi, the lattice mismatch between $In_xGa_{1-x}N$ and GaN leads to the effect that the indium mole fraction x becomes small at the initial growth stage of $In_xGa_{1-x}N$ grown on the GaN and AlGaN epitexial layers, whereas the crystalline quality deteriorates and

the indium mole fraction increases, by increasing the layer thickness (see page 24, last paragraph, and page 25, first paragraph).

This means that in the vicinity of dislocations, that is to say in the regions of lower thickness, the indium mole fraction is higher than in the regions of greater thickness. As the band of $In_xGa_{1-x}N$ becomes smaller with an increasing indium mole fraction, this results in an attractive potential in the vicinity of dislocations whereas contrastingly, according to the present invention, a shielding energy barrier exists there.

Due to this attractive potential created by Kawaguchi in the vicinity of dislocations, charge carriers can diffuse to the dislocations and thus possible non-radiating recombination of electron-hole pairs can appear at these dislocations. Therefore, the object of the present invention which is to provide a method for fabricating a light-emitting device which has an improved light yield, cannot be achieved in this way.

Consequently, a person skilled in the art would not come to the present invention, following the teaching of Kawaguchi.

The feature of forming a shielding energy barrier as explained above is not disclosed in Kawaguchi. Therefore, claim 1 is not anticipated by this reference. Moreover, Kawaguchi includes no teaching, suggestion or even a hint of this feature, nor is there any apparent motivation for a person with ordinary skill in the art to modify Kawaguchi to include this feature. Consequently, claim 1 is unobvious thereover. Thus, claim 1 is allowable over Kawauchi both under 35 USC 102 and 35 USC 103.

Mukai has been considered but found incapable of bridging the above-described gap between claim and Kawaguchi. Thus, claim is allowable over the combination of Kawaguchi and Mukai.

Each of claims 2-17 and 34 depends from claim 1 and, thus, is allowable therewith. Moreover, each of these claims includes features which to even more clearly distinguish each claim over the applied reference.

Based on all of the above, it is respectfully submitted that the present application is in condition for allowance. Prompt and favorable action to this effect is respectfully solicited.

It is believed that no fees or charges are required at this time in connection with the present application. However, if any fees or charges are required at this time, they may be charged to our Patent and Trademark Office Deposit Account No. 03-2412.

Respectfully submitted,
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Dated: July 27, 2006